ABSTRACT OF THE DISCLOSURE

A bus structure is implemented within a control chipset between a first control chip and a second control chip, comprising a first AD bus and a second AD bus. According to an arbitration method implemented to allow a dynamic adjustment of the direction of the AD buses transmission, the first control chip has a higher access priority in respect of the first AD bus, while the second control chip has a higher access priority in respect of the second AD bus. When the load of the first AD bus driving by the first control chip is high, a request signal is transmitted from the first control chip to the second control chip, so that if the second control chip is not currently using the second AD bus, the ownership of the second AD bus is handed over to the first control chip to improve the transmission efficiency, and vice versa.